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A 22nm and 16nm CMOS Implementation of Low Power and High-Speed Hybrid Logic Full Adder using High Performance 10-T XOR-XNOR Cell along with Design of 4-bit Binary Multiplier

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ABSTRACT: In the present arithmetic technology, the approach that is widely used in completing one full adder circuit is the hybrid logic. The efficiency of this hybrid logic in designing the full adder is obtained by using XOR-XNOR circuit. In this paper, a 4-bit binary multiplier is designed with the help of four different full adder designs. The proposed method was simulated in Tanner tool using 22nm and 16nm CMOS technology. The proposed multiplier circuit has a reduction in the terms of power for 12.91% and up to 68.99% and also in terms of area was 47.36% and up to 73.92% under 16nm and 22nm CMOS process technology. In the applicational view, the proposed multipliers are used for fast computational calculations and also digital signal processing applications to perform the various algorithms.

KEYWORDS: Hybrid logic, CMOS Technology, Digital Signal Processing Applications.

I. INTRODUCTION

NOWADAYS, portable electronic gadgets, such as cellular phones, personal digital assistants (PDAs), and notebook, form the integral part of life. For harnessing best out of these electronic systems, designers strive for small size, high speed, and energy-efficient circuits. These electronic systems mostly comprise arithmetic circuits. An adder is a fundamental component of most of the arithmetic circuits such as multipliers. These arithmetic circuits are extensively used in the data paths consuming almost one-third of power in the high-performance microprocessors. Therefore, enhancing the performance of the adders improves the performance of the whole system significantly [1]–[4]. To realize a full adder (FA) circuit, several static CMOS logic styles have been presented [3]–[5]. These logic styles can be broadly classified into two categories: classical design style and hybrid design style [8]. In classical design style, the FA is designed in a single module using MOS transistors. The complementary CMOS (C-CMOS) FA is an example of this approach. This design uses 28-transistors to realize pull-up and pull-down networks of a FA. It provides full swing outputs and robustness against voltage scaling and transistor sizing. The main drawback of this circuit is high input capacitance as each of the input is connected to the gates having at least a pMOS and an nMOS transistor which degrades the speed of the adder. Another example of the classical approach is complementary pass-transistor logic (CPL) FA. This structure provides high speed, full swing output, and good driving capability because of the high-speed differential stage, cross-coupled pMOS structure, and static inverter at the output. However, the power dissipation of this circuit is high due to a large number of internal nodes in the circuit. Also, the layout of this circuit is not symmetrical because of irregular transistor.

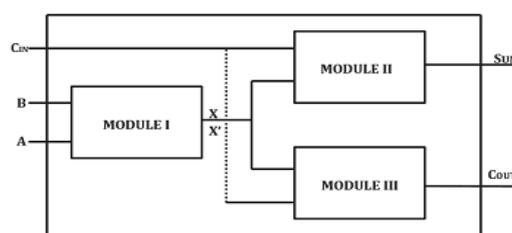


Figure 1 : Block Diagram of Hybrid logic FA Circuit



In the classical approach, FA can also be designed using pass transistors [6]. However, the pass transistors have an inherent threshold voltage drop problem. When logic “1” and logic “0” are passed through nMOS and pMOS, respectively, full swing logic “1” and logic “0” are not obtained at the output. To resolve this issue, a transmission gate (TG)-based approach has been developed. In this style, an nMOS transistor and a pMOS transistor are connected in parallel and controlled by complementary control signals. These pMOS and nMOS are turned on simultaneously and provide paths to both the logic (logic “1” and logic “0”) to provide full swing outputs. TG-based adder consumes low power; however, it has weak driving capability. Performance of this circuit can be enhanced by using the buffer at the output.

In this design, two complementary feedback transistors are used to restore the weak logic in complementary output nodes (XOR and XNOR) when both the inputs have same values (either “00” or “11”). This circuit suffers from the high worst case delay for the inputs “11” or “00” as in these cases; outputs reach their final voltage levels in two steps. This issue of slow response is resolved by Chang et al. who used two additional nMOS and pMOS transistors at the XOR and XNOR output nodes, respectively. This circuit provides good driving capability and full output swing. However, the cross-coupled structure adds an extra parasitic capacitance to the XOR–XNOR output nodes.

II. EXISTING METHOD

In a recent arithmetic technology, a hybrid logic style is commonly used to introduce complete full adder circuits. The efficiency of the XOR–XNOR circuit determines the performance of the hybrid full adder [11] in terms of delay, power and driving capability. In this paper presents a high speed low power 10-T XOR–XNOR circuit with full swing outputs and enhanced delay efficiency. The proposed method was simulated in Tanner tool using 22nm and 16nm CMOS technology. This proposed method also designed four different full adder design that makes use of the proposed XOR–XNOR circuit and usable sum and carry modules. In the terms of power delay product. The proposed full adder was embedded in 8-Bit cascaded full adder architecture to test their driving capabilities.

In recent years, various approaches to design XOR–XNOR circuit are presented which are discussed in Section 1. An XOR–XNOR circuit which provides full swing outputs using only six transistors is shown in Fig. 2(a). This configuration is realized using the CPL logic and feedback restorer transistors. It provides good delay performance for the inputs AB: “01” and “10.” However, a switching delay arises at the output for the inputs AB: “11” and “00.” The issue of higher delay for these inputs is resolved by the method used by Naseri and Timarchi [15] by adding 2 nMOS and 2 pMOS transistors in the circuit as shown in Fig. 2(b). The latter design not only resolves the problem of slow response but also reduces the power consumption of the circuit. However, it uses A as an input which needs an extra inverter. A new XOR–XNOR circuit is proposed in this section, which generates the inverted input internally without using any external inverter. This arrangement not only reduces the number of transistors in the circuit but also the number of internal nodes which reduces the overall delay and power consumption of the XOR–XNOR circuit.

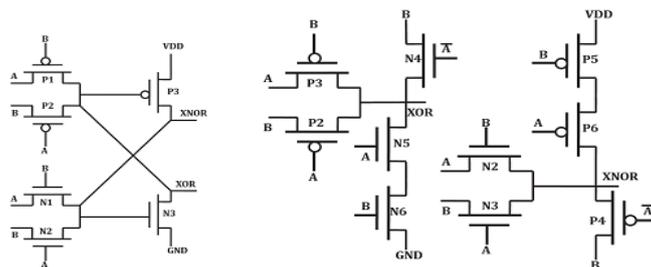


Figure 2 : XOR–XNOR circuits

The proposed XOR–XNOR circuit using ten transistors (10-T) is shown in Fig. 3. The proposed XOR–XNOR circuit is based on CPL and cross-coupled structure. It uses two pMOS (P1 and P2) and three nMOS (N3, N4, and N5) transistors at the XOR output side and two nMOS (N1 and N2) and three pMOS (P3, P4, and P5) at the XNOR output side. At the XOR side, P1 and P2 are connected in parallel as PTL [10], N4, and N5 as a restorer to provide a full swing output and N3 as feedback transistor. Similarly, at the XNOR output side N1 and N2 transistors are connected in parallel as PTL, P4, and P5 as a restorer to provide a full swing output and the P3 as a feedback transistor. This circuit provides full swing XOR–XNOR outputs simultaneously.



For understanding the operation of the proposed design, charging and discharging paths for XOR and XNOR outputs are shown in Table I. It includes all the paths which provide partial swing and full swing at the output nodes. For the input AB: “01,” the transistors P2, N1, and P4 turn on. Transistors P2 and N1 pass logic “1” and logic “0” at XOR and XNOR outputs, respectively, while transistor P4 turns on the transistor P3 to pass the weak logic “0” ($-V_{thp}$) at the XNOR output. Similarly, for the input AB: “10,” transistors P1, N2, and N4 turn on. Transistors P1 and N2 pass logic “1” and logic “0” at XOR and XNOR outputs, respectively, and transistor N4 turns on the transistor N3 which passes the weak logic “1” ($V_{DD}-V_{thn}$) at the XOR output. For these inputs (AB: “01” and “10”), the weak logic outputs will not affect the output swing as paths are available for full swing outputs.

For the input AB: “00,” the transistors P1, P2, P4, and P5 turn on. P1 and P2 pass weak logic “0” ($-V_{thp}$) at the XOR output, while P5 and P4 pass full logic “1” at XNOR output and the internal node X. Logic “1” at node X turns on the transistor N3 and a strong logic “0” is passed at the XOR output to make it full swing. Similarly, for input AB: “11,” transistors N1, N2, N4, and N5 turn on. The transistors N1 and N2 pass weak logic “1” ($V_{DD}-V_{thn}$) for the XNOR output, while the XOR node discharges completely through N4 and N5 [13]. Logic “0” also passes to the internal node X, which causes transistor P3 to be turned on and passes the full logic “1” at the XNOR output.

2.1 Proposed Multiplier Design:

In this proposed method, mainly the four full adder design which was present on the existing design were re-modified. Those re-modified circuits were done under 22nm and 16nm CMOS Process Technology. With the advancement of the designs, we can drastically reduce the power and delay and also mainly the performance of the circuits.

To understand in a brief, let us take one circuit for explanation:

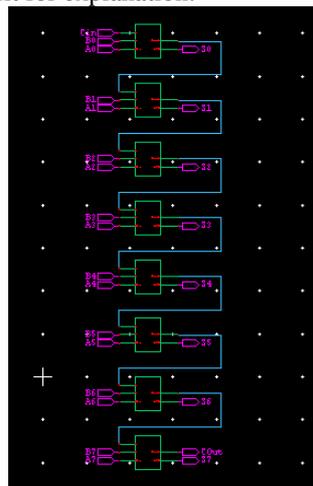


Figure 5. Full Adder design-2 8-bit in size under 22nm CMOS process technology

The above circuit is Full Adder design-2 8-bit in size under 22nm CMOS process Technology which is consider as our example for explanation. Here, the 1-bit full adder design [13] was converted into test bench circuit and these designs are used for 8-bit full adder designs.

So, here in the above circuit, there are 8 1-bit full adder circuits that are to be cascaded one by one. Here the input of first one-bit full adder was given as A1,B1. With this the operation was done and Sum and carry are obtained as outputs. So, the carry is propagated to second 1-bit full adder circuit as input and the same thing can be done to complete 8 1-bit full adder circuits [14]. With the help of propagation, the circuit becomes stabilized to store many inputs and performance increases.

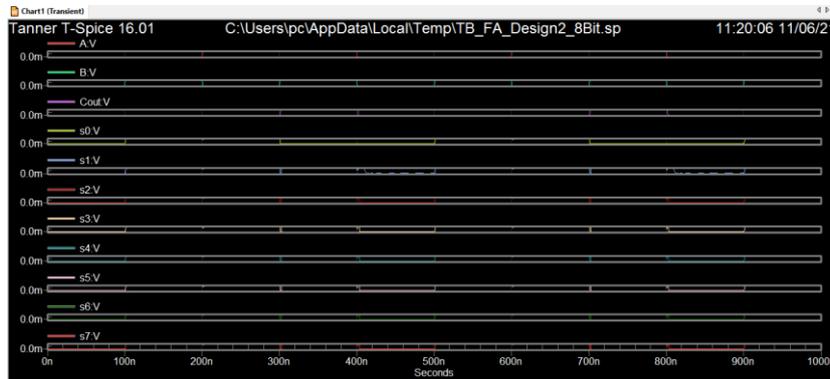


Figure6. test bench wave form for the circuit of 8-bit full adder design-2.

To understand this consider A,B as input and the outputs obtained when we applied A and B to the circuit are Cout and s0. The operation was quite simple which means when A=0, B=0 then the outputs was s0=0 and Cout=0; for the same circuit when we applied different inputs such as
 A=0,B=1 then outputs are s0=1 and Cout=0;
 A=1,B=0 then outputs are s0=1 and Cout=0;
 A=1,B=1 then outputs are s0=1 and Cout=1;
 This process continues till it execute the last 1-bit full Adder test bench circuit and obtains the output as s7 and c7. But in this we are just showing only sum outputs. Likewise, the same happens for remaining three designs like Full Adder design-1,3 and 4 under 22nm and 16nm CMOS Process Technology.

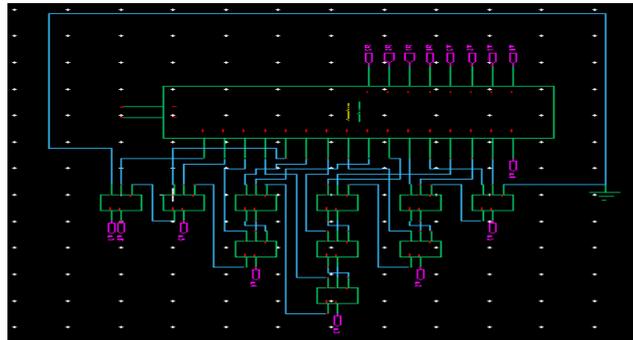


Figure 7 MULTIPLIER circuit for Full Adder design-1 under 16nm CMOS Technology.

Explanation of the above 4-bit MULTIPLIER circuit using Full Adder design-1:

Here, the above MULTIPLIER circuit needs 1 8-bit Full Adder Test Bench design and 8 1-bit Full Adder Test Bench designs. From the above circuit it was observed that, by the name 8-bit Multiplier circuit, we need 8 inputs such as A0, A1, A2, A3 and B0, B1, B2, B3.

With the inputs, the output s0 is obtained using 1-bit Full Adder test bench design. Here, the c0(carry element) was propagated to 2nd 1-bit Test bench design and the output is processed as s1 and c1. The same scenario, that c1 is propagated to 3rd 1-bit test bench design and processes the circuit and obtained the output as s2 and c2. This process continues until it covers all the eight 1-bit test bench designs which uses a common 8-bit Full adder test bench design circuit, which is like same as the designing of 8-bit full adder circuit using 1-bit Full adder design.



Figure 8 Test bench wave form for the 4-bit MULTIPLIER design

The same designs are projected and executed under 16nm CMOS Process Technology but here the difference between them was the process parameters and their predefined values. Here the comparison table for the single bit Full adder design as shown below:

The same designs are projected and executed under 16nm CMOS Process Technology but here the difference between them was the process parameters and their predefined values. Here the comparison table for the single bit Full adder design as shown below:

COMPARISON TABLES:

Comparisons of High Speed Hybrid Logic Full Adder Using High Performance 10T XOR XNOR Cell								
	Full Adder Design 1		Full Adder Design 2		Full Adder Design 3		Full Adder Design 4	
Technology	16 nm	22 nm						
MOSFETs	20	20	24	24	20	20	22	22
Area (nm)	320	440	384	528	320	440	352	484
Input Voltage (V)	0.5	0.9	0.9	0.9	0.5	0.9	0.9	0.9
Power (uW)	0.0457	0.269	0.206	0.423	0.0452	0.273	0.111	0.317

Comparisons of High Speed Hybrid Logic 8-Bit Full Adder Using High Performance 10T XOR XNOR Cell								
	8-Bit Full Adder Design 1		8-Bit Full Adder Design 2		8-Bit Full Adder Design 3		8-Bit Full Adder Design 4	
Technology	16 nm	22 nm						
MOSFETs	160	160	192	192	160	160	176	176
Area (um)	2.560	3.520	3.072	4.224	2.560	3.520	2.816	3.872
Input Voltage (V)	0.5	0.9	0.9	0.9	0.5	0.9	0.9	0.9
Power (uW)	0.424	1.886	1.769	4.646	1.280	3.281	0.612	2.049



Comparisons of High Speed Hybrid Logic 4-bit Binary Multiplier design Using High Performance 10T XOR XNOR Cell								
	Full Adder Design 1		Full Adder Design 2		Full Adder Design 3		Full Adder Design 4	
Technology	16 nm	22 nm						
MOSFETs	296	296	336	336	296	296	316	316
Area (um)	4.736	6.512	5.376	7.392	4.736	6.512	5.056	6.952
Input Voltage (V)	0.5	0.9	0.9	0.9	0.5	0.9	0.9	0.9
Power (uW)	1.619	4.431	2.408	6.899	1.717	4.777	1.291	3.634

From the above comparison table, we know that for all the full adder designs using 16nm CMOS Process Technology has a huge reduction of Power compared to 90nm CMOS Process Technology based on existing method.

Advantages:

- Less Voltage Drop Problems
- More speed and more energy efficient circuits
- High performances

III. CONCLUSION

In this project, a new multiplier designs was proposed based on 16nm and 22nm cmos process technology under four full adder circuit designs using the XOR-XNOR circuits. Using the proposed XOR-XNOR circuit, four new FA cells based on hybrid logic design style were also proposed. The performance of the proposed multiplier design based on XOR-XNOR circuit and the FA cells was tested by simulating it with the tanner EDA tool using 16nm and 22nm CMOS Process Technology. The proposed multiplier design showed a reduction in terms of area was 47.36% and up to 73.92% under 16nm and 22nm technology and also reduction in terms of power for 12.91% and up to 68.99% under 16nm and 22nm technology. This power was reduced drastically when compared with the existing method implementation. The performance of the FA cells and proposed multiplier designs was also tested under cascaded connections. From this we observed that the performance of proposed Multiplier design using Full Adder design-4 works efficiently under 16nm and 22nm process technology when compared with other Full Adder designs. In the application view, the proposed multipliers are used for fast computational processes and also digital signal processing applications which requires faster calculations.

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